Docket No. AUS920010118US1

ABSTRACT OF THE DISCLOSURE

PRACTICAL METHODOLOGY FOR EARLY BUFFER AND WIRE RESOURCE ALLOCATION

A method, system, and computer program product for
5   allocating buffer and wire placement in an integrated
circuit design is provided. In one embodiment, the
surface of a integrated circuit design is represented as
a tile graph. Allocation of buffer locations for
selected tiles in the tile graph is then received and
10   nets are routed between associated sources and sinks.
Buffer locations within selected tiles are then
selectively assigned based upon buffer needs of the nets,
wherein the nets are routed through selected tiles and
assigned buffer locations using a cost minimization
15   algorithm.